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EXAMINER	
TSAI, HENRY	
ART UNIT	**PAPER NUMBER**
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/779,886	Applicant(s) MOYER, WILLIAM C.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-11, 14-16, 18, 20, and 23* is/are rejected.

7)☒ Claim(s) *5,12,13,17,19,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ___ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2-4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 3, 4, 14, 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, line 2, and claim 12, line 2, it is not clear which "value" is referred to since more than one values were mentioned in claim 1.

In claim 14, line 1, "the change of control" and line 2, "the means for executing" lack proper antecedent basis since they were not defined previously.

In claim 15, line 1, "the change of control" lacks proper antecedent basis since it was not defined previously.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 6, 7, 18, 20 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Emma et al. (USP 5,434,985), hereafter referred to as Emma et al.

Referring to claims 1 and 23, Emma et al. discloses, as claimed, a method of program execution in a data processing system (203, see Fig. 2) comprising: means for fetching (see Col. 10, lines 49-50, and PFAR 402 see Fig. 4) a first instruction (see Fig. 3, the first instruction is at address B+b, conditional branch if <cond> Go to C) located at a first address (B+b); and means for executing (203, superscalar processor, see Fig. 2) the first instruction with the data processing system, the method comprising: executing the first instruction (see Fig. 3, the first instruction is at address B+b, conditional branch if <cond> Go to C as set forth); selecting a jump address based upon a value (inherently, a first value in the condition of the conditional branch, such as when I-J > 0 is the condition) by

providing a second address (address C as shown in Fig. 3) for the jump address if a comparison of the value with a predetermined value (when I-J > 0 is the condition, and the 0 is the predetermined value) has a first result (the result when I-J >0), and providing a third address (the address not contiguous to address B+b, when there is an address gap therebetween see Fig. 3, also note the addresses between two instructions are not necessary to be contiguous when saved in the system's memory) for the jump address if the comparison of the value with the predetermined value has a second result (when I-J $\leq$ 0), wherein neither the second address nor the third address is contiguous to the first address (since the second address C is not contiguous to address B+b, and for the third address is not contiguous to address B+b as explained above); and always implementing a change of control in the program execution in response to executing the first instruction by redirecting program execution to the jump address.

As to claim 2, Emma et al. also discloses the first result is a comparison determination that the value is greater than the predetermined value(when I-J > 0 is the condition) and the second result (when I-J $\leq$ 0 is the condition) is a comparison determination that the value is less than or equal to the predetermined value (the 0 is the predetermined value).

As to claim 3, Emma et al., as best understood, also discloses: implementing the value as a count value stored in a counter (since a counter inherently storing a count value in the Emma et al.'s system during the process).

As to claim 6, Emma et al. also discloses: selecting the second address and the third address to be within a predetermined range of addresses that is less than a total range of addresses within the data processing system (Note this step is inherent since the selected addresses should be in the range of addressable space in the Emma et al.'s system).

As to claim 7, Emma et al. also discloses: selecting the second address to be within a predetermined range of addresses that is less than a total range of addresses within the data processing system (as set forth above, this step is inherent since the selected addresses should be in the range of addressable space in the Emma et al.'s system).

As to claim 18, Emma et al. also discloses: a data processing system comprising: a memory (inherently existing in the Emma et al.'s system, such as main memory or instruction cache) for storing a plurality of program instructions; a processor (203, see Fig. 2, superscalar processor of the Emma et al.'s system) coupled to the memory via a data bus for fetching the program instructions from the memory and selectively

executing the plurality of program instructions (see Fig. 3); and a storage device for storing a plurality of processing instructions to be executed by the processor (203, see Fig. 2, superscalar processor of the Emma et al.'s system), the plurality of processing instructions arranged in groups wherein each group is correlated to a predetermined one of the plurality of program instructions; the processor (203, see Fig. 2, superscalar processor of the Emma et al.'s system) executing a predetermined processing instruction at a predetermined address (see Fig. 3, the instruction is at address B+b, conditional branch if <cond> Go to C as set forth) and selecting a jump address based upon a value (inherently, a first value in the condition of the conditional branch, such as when I-J > 0 is the condition) by providing a first address (address C as shown in Fig. 3) for the jump address if a comparison of the value with a predetermined value (when I-J > 0 is the condition, and the 0 is the predetermined value) has a first result, and by providing a second address (the address not contiguous to address B+b, when there is an address gap therebetween see Fig. 3, also note the addresses between two instructions are not necessary to be contiguous when saved in the system) for the jump address if the comparison of the value with the predetermined value has a second result, wherein neither the first address nor the second

addresses is contiguous to the predetermined address, execution of the predetermined processing instruction always implementing a change of control in program execution.

Referring to claim 20, Emma et al. also discloses: the processor (203, see Fig. 3) further comprises: an instruction register for receiving the program instructions; an instruction decoder (inside 293, see Col. 10, lines 10-11) coupled to the instruction register for decoding the program instructions into specific opcode values; a control circuit (inherently existing inside 203) coupled to the instruction decoder for providing control signals in response to the specific opcode values; address generation circuitry (inherently existing inside 203, see Fig. 2, superscalar processor of the Emma et al.'s system) coupled to the control circuit for receiving the control signals and creating the jump address; registers (inherently existing inside 203, the superscalar processor of the Emma et al.'s system see Fig. 2) coupled to the address generation circuitry for storing operands in response to the control circuit; and an arithmetic logic unit (inherently existing inside 203, the superscalar processor of the Emma et al.'s system see Fig. 2) coupled to the address generation circuitry and the control circuit, the arithmetic logic unit processing the operands stored by the registers.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 10, and 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al. in view of Stallings, Willian, "Computer Organization and Architecture", pages 581-583, 5th edition, 1999, hereafter referred to as Stallings.

Emma et al. discloses the claimed invention except for: providing a storage device having a predetermined range of addresses for storing processing instructions to be executed by the means for executing, the processing instructions arranged in groups, each group correlated to a predetermined opcode of a program (claim 8); structuring the storage device in sections of a predetermined number of instruction slots, a predetermined amount of each of the sections dedicated to storage of the

instructions (claim 10); directing execution of the processing instructions from one of the sections of the storage device to an address outside of the predetermined range of addresses and subsequently redirecting program execution back to a predetermined portion of another one of the sections of the storage device (claim 12); and providing a storage device having a predetermined range of addresses for storing processing instructions arranged in groups, at least two of the groups having differing numbers of processing, instructions and thus differing sizes (claim 16).

However, Stallings discloses: providing a storage device (a control memory, see Fig. 15.2) having a predetermined range of addresses (the control memory, see Fig. 15.2, having a predetermined range of address space) for storing processing instructions (the microinstructions saved in a control memory)to be executed by the means for executing, the processing instructions arranged in groups (specific operation routines, such as AND, ADD , and IOF routines shown in Fig. 15.2), each group correlated to a predetermined opcode of a program; structuring the storage device (the control memory, see Fig. 15.2, having a predetermined range of address space) in sections of a predetermined number of instruction slots (specific operation routines, such as AND, ADD , and IOF routines shown in

Fig. 15.2), a predetermined amount of each of the sections (specific operation routines, such as AND, ADD , and IOF routines shown in Fig. 15.2) dedicated to storage of the instructions; and directing execution of the processing instructions from one of the sections of the storage device to an address outside of the predetermined range of addresses and subsequently redirecting program execution back to a predetermined portion of another one of the sections of the storage device (such as a subroutine call when reaching a return instruction and control flow inside the control memory, as set forth, comprising the microinstructions including "jump"; and specific operation subroutines, as Fig. 15.2); and providing a storage device having a predetermined range of addresses for storing processing instructions arranged in groups (specific operation routines, such as AND, ADD , and IOF routines shown in Fig. 15.2), at least two of the groups having differing numbers of processing, instructions and thus differing sizes (the specific operation routines, such as AND, ADD , and IOF routines having differing numbers of processing, instructions and differing sizes see Fig. 15.2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Emma et al.'s system to comprise providing a storage device having a predetermined range of addresses for storing processing

instructions to be executed by the means for executing, the processing instructions arranged in groups, each group correlated to a predetermined opcode of a program; structuring the storage device in sections of a predetermined number of instruction slots, a predetermined amount of each of the sections dedicated to storage of the instructions; directing execution of the processing instructions from one of the sections of the storage device to an address outside of the predetermined range of addresses and subsequently redirecting program execution back to a predetermined portion of another one of the sections of the storage device; and providing a storage device having a predetermined range of addresses for storing processing instructions arranged in groups, at least two of the groups having differing numbers of processing, instructions and thus differing sizes, as taught by Stallings, in order to increase the flexibility and scalability for controlling the data processing for the Emma et al.'s system.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al. in view of Stallings as applied to claims 8, 10, 11, and 16 above, and further in view of Griesemer (USP 6,021,273).

Emma et al. in view of Stallings discloses the claimed invention except for the opcode being a Java bytecode. Griesemer teaches to use the opcode being a Java bytecode (101, see Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Emma et al./Stallings's system to comprise the opcode being a Java bytecode, as taught by Griesemer, in order to obtain the portability for the platform independent feature thereof.

Allowable Subject Matter

7. Claims 4, 14, and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 5, 12, 13, 17, 19, 21, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Scalzi et al. discloses preprocessing of stored target routines for emulating incompatable instructions on a target processor; Thusoo et al. also discloses a system and method providing hardware support for fast software emulation of unimplemented instructions; Davis et al. discloses a memory system having next instruction buffer which stores target tracks of jumps prior to CPU access of instruction; Hemdal et al. teaches method for execution of jump in an instruction memory; Yamamoto et al. discloses a processor which returns from a subroutine at high speed and a program translating apparatus which generates machine programs making a high speed return form a subroutine; and Bala teaches using a virtual machine to execute Java Bytecodes. All above references disclose some limitations similar to the claimed invention.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can

normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

April 5, 2004